REMARKS

Claims 1-12 were previously pending in this application. By this amendment, Applicants are canceling claim 3 without prejudice or disclaimer. Claims 1, 8, 10, and 12 have been amended. New claims 13-18 have been added. As a result claims 1-2 and 4-18 are pending, with claims 1, 8, and 10 being independent claims. No new matter has been added.

I. Information Disclosure Statement

The Office Action states that the Information Disclosure Statement (IDS) filed on May 14, 2001 did not include a copy of the second citation. Applicants are submitting herewith an IDS citing each previously cited reference and enclosing a copy of each cited reference. As the previously cited applications have now issued as patents, the issued patents are cited. The Examiner is respectfully requested to consider the cited references, and initial and return the associated Form 1449.

II. Drawings

The Office Action states that "the input capacitor comprising a capacitor array as claimed in claim 3 must be shown or the feature(s) canceled from the claim(s)." Claim 3 has been canceled without prejudice or disclaimer. Accordingly, withdrawal of this rejection is respectfully requested.

III. Claim Rejections Under 35 U.S.C. §112

Claim 3 is rejected as allegedly failing to comply with the written description requirement. Claim 3 has been canceled without prejudice or disclaimer. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Claim Rejections Under 35 U.S.C. §102

Claims 1-7 and 9-12, which include independent claims 1, 9, and 10, are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,342,919 ("Opris"). Claims 1, 9, and 10 have been amended to clearly distinguish over Opris.

a. Discussion of Opris

Opris discloses an amplifier circuit comprising a first signal path 1 for green pixels and a signal path 2 for red and blue pixels (Col. 3, lines 21-22, 26-28 and 32-33). The gain of the first signal path 1 is established by a combination of capacitors C1, C2, CA, and CB (Col. 3, lines 21-24). The gain of the second signal path 2 established by a combination of capacitors C3, C4, CC, CD (Col. 3, lines 26-29). The path used for input pixels alternates between signal path 1 and signal path 2 and is switched according to the sampling rate (Col. 3, lines 12-14).

b. Claim 1

Claim 1 has been amended to recite a pixel gain amplifier circuit comprising, inter alia, a feedback capacitor, coupled between the input and the output of the amplifier, *that samples a reference voltage during the first time phase* and receives charge from the input capacitor during the second time phase. The amendment to the claim is supported, e.g., at page 5, lines 27-29 of the present application.

Opris discloses, at line 67 of column 2 to line 18 of column 3, that during a first clock phase, an input signal is sampled onto capacitors C1, C2, CA, and CB. During a second clock phase, capacitors C1 and CA are connected between an inverting input and an output of op amp 200, while capacitors C2 and CB are connected between the inverting input and ground. Also during the second clock phase, an input signal is sampled onto capacitors C3, C4, CC, and CD. During the first clock phase, capacitors C3 and CC are connected between the inverting input and the output of op amp 200, while capacitors C4 and CD are connected between the inverting input and ground.

Thus, although Opris discloses capacitors (C1 and CA, C3 and CC) that may be coupled between an input and an output of op amp 200, these capacitors do not sample a reference voltage. Rather, these capacitors sample an input voltage during one phase, and are coupled between the input and output of op amp 200 during an alternate phase. In view of the foregoing, Opris does not disclose a feedback capacitor, coupled between the input and the output of the amplifier, *that samples a reference voltage during the first time phase* and receives charge from the input capacitor during the second time phase, as recited in claim 1. Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. §102(e) is respectfully requested.

Claims 2, 4-8, 13, and 17-18 depend from claim 1 and are allowable for at least the same reasons.

c. Claim 9

Claim 9 has been amended to recite a method of amplifying input pixels comprising, inter alia, a step of controlling a gain of the amplification for each pixel *in response to a gain control signal comprising information related to a desired gain.* The amendment to the claim is supported, e.g., at page 6, lines 4-8 of the present application.

In the amplifier circuit of Opris, the gain is established for each signal path based on the capacitor combination of each signal path. Thus, a first gain is associated with the first signal path 1 and a second gain is associated with the second signal path 2 (Col. 3, lines 16-18). The signal path that is used to amplify the input signal is switched between the first and second signal paths by clock signals $\phi 1$ and $\phi 2$ that control switches of the amplifier circuit (Col. 2, lines 61-64).

In view of the foregoing, Opris does not disclose a step of controlling a gain of the amplification for each pixel *in response to a gain control signal comprising information related to a desired gain*, as recited in claim 9. Accordingly, withdrawal of the rejection of claim 9 under 35 U.S.C. §102(e) is respectfully requested.

d. Claim 10

Claim 10 has been amended to recite a pixel gain amplifier circuit comprising an amplifier having an input, an output and a gain, and *means for varying the gain of the amplifier from a first gain for a first pixel to a second gain for a second pixel, wherein the first and second gains are determined, at least in part, by an input capacitor and a feedback capacitor*. The amendment to the claim is supported, e.g., at page 5, line 24 – page 6, line 8 and Figure 8.

As discussed previously, in the amplifier circuit of Opris, a first signal path 1 is used for green pixels and a signal path 2 is used for red and blue pixels (Col. 3, lines 21-22, 26-28 and 32-33). The gain of the first signal path 1 is established by a combination of capacitors C1, C2, CA, and CB (Col. 3, lines 21-24). The gain of the second signal path 2 established by a combination of capacitors C3, C4, CC, CD (Col. 3, lines 26-29). The path used for input pixels alternates between signal path 1 and signal path 2 and is switched according to the sampling rate (Col. 3, lines 12-14). Thus, in Opris, the gain for a first pixel is established by the combination of a first group of capacitors and the gain for a second pixel is established by the combination of a second group of capacitors that are distinct from the first group of capacitors.

In view of the foregoing, Opris does not disclose a pixel gain amplifier circuit comprising means for varying the gain of an amplifier from a first gain for a first pixel to a second gain for a second pixel, wherein the first and second gains are determined, at least in part, by an input capacitor and a feedback capacitor, as recited in claim 10. Accordingly, withdrawal of the rejection of claim 10 under 35 U.S.C. §102(e) is respectfully requested.

Claims 11-12 and 14-16 depend from claim 10 and are allowable for at least the same reasons.

III. Claim Rejections Under 35 U.S.C. §103(a)

Claim 8 is rejected under 35 U.S.C. §103(a) as being obvious over Opris in view of U.S. Patent No. 6,166,766 (Moore et al.). Claim 8 depends from independent claim 1 and is believed to be allowable for at least the same reasons as claim 1. Accordingly, for the sake of brevity, Applicants believe that it is unnecessary at this time to argue the allowability of claim 8 and

reserve the right to specifically address the patentability of this claim in the future, if deemed necessary.

IV. Claim Rejections Under 35 U.S.C. §101

Claims 1, 2, 5, and 8 are rejected under 35 U.S.C. §101 as claiming the same invention as that of claims 1, 2, 3, and 4, respectively, of prior U.S. Patent No. 6,433,632 ("Nakamura").

MPEP §804 discusses the following test for determining whether a statutory double patenting rejection is proper:

> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice? 35 U.S.C. 101 prevents two patents from issuing on the same invention. "Same invention" means identical subject matter. *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957)

Thus, claims must recite identical subject matter for a statutory double patenting rejection to be proper.

Claim 1 of Nakamura (and hence claims 2-4, which depend therefrom) recites limitations not present in claims 1, 2, 5, or 8 of the present application. For example, the claim recites "wherein no sampling switch is located between the input capacitor and the input terminal." As this recitation limits the scope of claim 1 of Nakamura in a manner in which claims 1, 2, 5, or 8 of the present application are not limited, none of claims 1, 2, 5, or 8 of the present application recite identical subject matter to any of claims 1-4 of Nakamura.

In view of the foregoing, withdrawal of the rejection of claims 1, 2, 5, and 8 under 35 U.S.C. §101 is respectfully requested.

V. New Claims

Claims 13-18 have been added to further define Applicants' contribution to the art. No new matter has been added. Claims 13 and 17-18 and claims 14-16 depend from independent claims 1 and 10, respectively, and are believed to be allowable at least on the basis of their dependency.

Conclusion

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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